Jialong Chen

che00184@umn.edu | University of Minnesota Twin Cities, MN, 55455

EDUCATION

University of California, Los Angeles — Los Angeles, CA
Master of Science 3.76/4.0 — **Sept. 2024 – Jun. 2026**

Xidian University & Heriot-Watt University — China & UK
BA, Engineering 3.9/4.0 — **Sept. 2020 - Jun. 2024**

- Awards & Honors: Deputy Principal's Award, Overseas Scholarship for Outstanding Graduates, The Third-class Scholarship

RESEARCH EXPERIENCE

University of California, Los Angeles — Los Angeles, CA
Statistical Yield Modeling for 3D-Stacked Hybrid-Bonded Systems — **Dec. 2025 – Jun. 2026**
Research Assistant (supervised by Prof. Puneet Gupta)

- Co-developed a comprehensive stage-aware yield-modeling framework for multi-layer D2D and W2W hybrid-bonded systems, integrating overlay, particle contamination, Cu recess, ESD, TSV defects, and stack warpage.
- Derived probabilistic first-contact and minimum-gap models under random die tilt, wafer bow, and Cu-pad variation, using Gaussian statistics and Gauss–Hermite quadrature to generate spatial ESD-risk heatmaps efficiently.
- Extended multilayer thin-film mechanics to incorporate initial die warpage, finite layer thickness, CTE mismatch, and sequential assembly, enabling analytical prediction of curvature, layer stress, and final-stack warpage distributions.
- Developed correlated statistical-yield formulations for both intermediate assembly steps and final stacks, avoiding inaccurate independence assumptions across sequential bonding constraints.
- Validated the analytical mechanics against large-scale ANSYS simulations, achieving 0.108 μm mean absolute error across 300 D2D cases without empirical fitting, and established that D2D warpage is dominated by initial die bow while W2W stacks are more sensitive to sequential bow ordering.

University of California, Los Angeles — Los Angeles, CA
Yield-Aware I/O Planning for Hybrid-Bonded Chiplets — **Jun. 2025 – Nov. 2025**
Research Assistant (supervised by Prof. Puneet Gupta)

- Developed the first layout-aware I/O planning framework for hybrid-bonded 2.5D/3D chiplet systems, jointly modeling ESD, particle contamination, overlay variation, and thermomechanical failures.
- Derived a statistical first-arcing ESD model incorporating die tilt, Cu-pad recess variation, CDM peak current, and device-level breakdown probability, validated through Monte Carlo simulation.
- Formulated ILP and scalable greedy optimization algorithms with redundancy, reach, and floorplanning constraints; achieved near-ILP solution quality with substantially improved runtime.
- Evaluated the framework on JEDEC HBM4 and million-bump multi-chiplet benchmarks, improving bonding yield by up to 19.9 percentage points without relocating physical bumps or increasing die area.
- Established practical design guidelines showing that critical I/Os should avoid die edges and corners, while redundant pads should be spatially separated to mitigate correlated bonding failures.

TECHNICAL SKILLS

- Programming Languages: C, C++, Verilog, Python, MATLAB, C#, HTML, JavaScript, SQL
- Hardware & Simulation Tools: ModelSim, Synopsys Design Compiler, Cadence Virtuoso & Innovus, Proteus, Ansys
- Applications: 2.5D/3D chiplet integration, hybrid bonding, advanced semiconductor packaging, ESD and thermomechanical reliability, stack warpage and bonding-yield modeling, yield-aware I/O planning