Jialong Chen

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EDUCATION

University of California, Los Angeles — Los Angeles, CA
Master of Science 3.767/4.0 — **Sept. 2024 – Jun. 2026**

Xidian University & Heriot-Watt University — China & UK
BA, Engineering 3.9/4.0 — **Sept. 2020 - Jun. 2024**

- Awards & Honors: Deputy Principal's Award, Overseas Scholarship for Outstanding Graduates, The Third-class Scholarship

RESEARCH EXPERIENCE

University of California, Los Angeles — Los Angeles, CA
Statistical Yield Modeling for 3D-Stacked Hybrid-Bonded Systems — **Dec. 2025 – Jun. 2026**
Research Assistant (supervised by Prof. Puneet Gupta)

- Co-developed a comprehensive stage-aware yield-modeling framework for multi-layer D2D and W2W hybrid-bonded systems, integrating overlay, particle contamination, Cu recess, ESD, TSV defects, and stack warpage.
- Derived probabilistic first-contact and minimum-gap models under random die tilt, wafer bow, and Cu-pad variation, using Gaussian statistics and Gauss–Hermite quadrature to generate spatial ESD-risk heatmaps efficiently.
- Extended multilayer thin-film mechanics to incorporate initial die warpage, finite layer thickness, CTE mismatch, and sequential assembly, enabling analytical prediction of curvature, layer stress, and final-stack warpage distributions.
- Developed correlated statistical-yield formulations for both intermediate assembly steps and final stacks, avoiding inaccurate independence assumptions across sequential bonding constraints.

University of California, Los Angeles — Los Angeles, CA
Yield-Aware I/O Planning for Hybrid-Bonded Chiplets — **Jun. 2025 – Nov. 2025**
Research Assistant (supervised by Prof. Puneet Gupta)

- Developed the first layout-aware I/O planning framework for hybrid-bonded 2.5D/3D chiplet systems, jointly modeling ESD, particle contamination, overlay variation, and thermomechanical failures.
- Derived a statistical first-arcing ESD model incorporating die tilt, Cu-pad recess variation, CDM peak current, and device-level breakdown probability, validated through Monte Carlo simulation.
- Formulated ILP and scalable greedy optimization algorithms with redundancy, reach, and floorplanning constraints; achieved near-ILP solution quality with substantially improved runtime.
- Evaluated the framework on JEDEC HBM4 and million-bump multi-chiplet benchmarks, improving bonding yield by up to 19.9 percentage points without relocating physical bumps or increasing die area.
- Established practical design guidelines showing that critical I/Os should avoid die edges and corners, while redundant pads should be spatially separated to mitigate correlated bonding failures.

Heriot-Watt University — Edinburgh, UK
Deep Learning–Based Low-Light Image and Video Enhancement — **Sept. 2023 - Apr. 2024**
Bachelor's Thesis (supervisor by Prof. Alexander Belyaev)

- Developed and evaluated a zero-reference low-light enhancement framework based on Zero-DCE and Zero-DCE++, reformulating image enhancement as pixel-wise illumination-curve estimation without requiring paired low-/normal-light training images.
- Proposed a channel-consistency loss based on KL divergence to preserve inter-channel relationships between input and enhanced images, suppress color shifts, noise, and ineffective features, and improve visual fidelity under nonuniform illumination.
- Implemented and trained the model in Python/PyTorch on an NVIDIA RTX 3060 GPU, resolving legacy CUDA and library compatibility issues and conducting 100 training epochs with a multi-objective reference-free loss formulation.
- Extended the image model to low-light video by developing a complete frame extraction, enhancement, and reconstruction pipeline, and demonstrated that the proposed Zero-DCE++ variant produced superior image and video quality compared with baseline Zero-DCE and Zero-DCE++.
- Demonstrated the feasibility of lightweight, reference-free enhancement for mobile and edge-vision applications, enabling fast image restoration without the high data-collection cost associated with supervised paired-image datasets..

TECHNICAL SKILLS

- Programming Languages: C, C++, Verilog, Python, MATLAB, C#, HTML, JavaScript, SQL
- Hardware & Simulation Tools: ModelSim, Synopsys Design Compiler, Cadence Virtuoso & Innovus, Proteus, Ansys
- Applications: 2.5D/3D chiplet integration, hybrid bonding, advanced semiconductor packaging, ESD and thermomechanical reliability, stack warpage and bonding-yield modeling, yield-aware I/O planning